LISTING OF CLAIMS:

1. (Currently Amended) A frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the frequency translating repeater comprising:

a detector circuit configured to detect if a signal is present on one of two frequency channels associated with the frequency translating repeater;

a frequency translator configured to change a frequency channel associated with the signal from the one of the two frequency channels to an other of the two frequency channels; ~~and~~

a gain control circuit for adjusting a gain of the signal; and

a delay circuit configured to add a delay to the signal to compensate for a signal detection interval, a gain adjustment interval and a transmitter configuration interval.

2. (Original) The frequency translating repeater according to claim 1, wherein the delay circuit includes an analog storage device.

3. (Original) The frequency translating repeater according to claim 1, wherein the delay circuit includes at least one surface acoustic wave filter configured for one or more of: analog signal storage and channel selection.

4. (Original) The frequency translating repeater according to claim 1, wherein the detector circuit includes a processor.

5. (Original) The frequency translating repeater according to claim 4, wherein the detector circuit further includes an analog detection circuit.

6. (Currently Amended) The frequency translating repeater according to claim 1, ~~further comprising a~~ wherein the gain control circuit ~~having~~ has one of a gain value and an attenuation value associated therewith.

7. (Original) The frequency translating repeater according to claim 6, wherein:

the detector is further for detecting a received signal strength of the signal, and

the gain control circuit is further for using the received signal strength of the signal to adjust a gain value of the signal.

8. (Original)The frequency translating repeater according to claim 7, wherein the gain control circuit is further for controlling at least one of the gain value and the attenuation value based on a predetermined criteria to achieve a specific signal transmit output power.

9. (Original)The frequency translating repeater according to claim 8, wherein the predetermined criteria is for modifying the specific signal transmit output power and includes at least one of the following: frequency separation between a receive frequency and a transmit frequency, a regulatory rule, a temperature, a received power level, a transmit power level, and a detected interference level.

10. (Currently Amended) The frequency translating repeater according to claim 8, further comprising:

an antenna for receiving the signal on one of the two frequency channels;

a RF splitter coupled to the antenna, the RF splitter for splitting the signal onto a first path and a second path;

first and second IF splitters disposed on the first and second paths, respectively, the first IF splitter for splitting the first path into a first IF signal path and a second IF signal path, the second IF splitter for splitting the second path into a third IF signal path and a fourth IF signal path,

wherein the detector circuit and the gain control circuit are located on the first IF signal path and the third IF signal path, wherein the delay circuit is located on the second IF signal path and the fourth IF signal path, wherein the detector circuit includes a processor, wherein the processor further includes a memory and wherein the predetermined criteria are stored in the memory.

11. (Original) A frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the frequency translating repeater comprising:

a detector circuit configured to detect if a signal is present on one of two frequency channels associated with the frequency translating repeater and to detect a received detected signal power of the signal;

a frequency translator configured to change a frequency channel associated with the signal from the one of the two frequency channels to an other of the two frequency channels;

a delay circuit configured to add a delay to the signal to compensate for a signal detection interval and a transmitter configuration interval; and

a gain control circuit configured to adjust a gain value of the signal at least in part based on the received detected signal power detected by the detector circuit.

12. (Original) The frequency translating repeater according to claim 11, wherein the gain control circuit is further configured to adjust the gain value based at least in part on criteria

including which of the one of the two frequency channels the signal is received on, and which of the other of the two frequency channels is changed to.

13. (Original) The frequency translating repeater according to claim 12, wherein the criteria further includes at least one of a regulatory rule for transmission, an operating temperature, and frequency separation between receive and transmit frequencies.

14. (Currently Amended) The frequency translating repeater according to claim [[~~11~~]] 12, wherein the criteria further includes a distance between a receive frequency and a transmit frequency, and wherein the automatic gain control circuit is further configured to apply more filtering to the signal based on the distance.

15. (Original) A frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the frequency translating repeater comprising:

a detector circuit configured to detect if a signal is present on one of two frequency channels associated with the frequency translating repeater;

a frequency converter configured to convert the signal from a radio frequency (RF) signal to an intermediate frequency (IF) signal;

a frequency translator configured to change a frequency channel associated with the IF signal from the one of the two frequency channels to an other of the two frequency channels;

a delay circuit configured to add a delay to the IF signal to compensate for a signal detection interval and a transmitter configuration interval; and

a gain control circuit configured to adjust a gain value of the IF signal.

16. (Original) The frequency translating repeater according to claim 15, wherein the gain control circuit is further configured to adjust the gain value of the IF signal at least in part based on a received detected signal power detected by the detector circuit.

17. (Currently Amended) The frequency translating repeater according to claim 15, further comprising:

an antenna for receiving the signal present on the one of two frequency channels;

a RF splitter coupled to the antenna, the RF splitter for splitting the signal onto a first path and a second path;

first and second IF splitters disposed on the first and second paths, respectively, the first IF splitter for splitting the first path into a first IF signal path and a second IF signal path, the second IF splitter for splitting the second path into a third IF signal path and a fourth IF signal path,

wherein the detector circuit is located on the first IF signal path and the third IF signal path,

wherein the delay circuit is located on the second IF signal path and the fourth IF signal path,

wherein ~~and~~ the gain control circuit ~~are~~ is located ~~respectively~~ on ~~a first and a second signal~~ the first IF signal path and the third IF signal path.

18. (Original) The frequency translating repeater according to claim 17, wherein the detector circuit includes a logarithmic amplifier and wherein the output of the logarithmic amplifier is coupled to the gain control circuit for control thereof.

19. (Original) The frequency translating repeater according to claim 18, wherein the detector circuit and the automatic gain control circuit each have different bandwidths.

20. (Original) The frequency translating repeater according to claim 19, wherein the automatic gain control circuit includes a processor and a memory storing a predetermined criteria and wherein the processor is configured to use the predetermined criteria to establish an offset gain value of the IF signal, resulting at least in part in a transmitter target output power independent of the detected receive power of the signal as detected by the detector circuit.

21. (Currently Amended) The frequency translating repeater according to claim 20, wherein the processor is further configured to:

convert the output of the logarithmic amplifier to a digital signal; and

establish the gain value of the IF signal using the digital signal.

22. (Currently Amended) A method for frequency translation in a frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the method comprising:

[[a]] detecting if a signal is present on one of two frequency channels associated with the frequency translating repeater;

changing a frequency channel associated with the signal from the one of the two frequency channels to an other of the two frequency channels; and

adding a delay to the signal to equivalent to a signal detection interval and a transmitter configuration interval.

23. (Original) The method according to claim 22, wherein the adding the delay includes delaying the signal in an analog storage device.

24. (Original) The method according to claim 22, wherein the adding the delay includes at delaying the signal in at least one surface acoustic wave filter configured for one or more of: analog signal storage and channel selection.

25. (Original) The method according to claim 24, wherein the detecting includes detecting in an analog detection circuit.

26. (Currently Amended) The method according to claim [[21]] 22, further comprising:

splitting the signal onto a first path and a second path;

splitting the first path into a first IF signal path and a second IF signal path, and splitting the second path into a third IF signal path and a fourth IF signal path,

setting a gain associated with the signal,

wherein the detecting if the signal is present further includes detecting if the signal is present on the first IF signal path or the third IF signal path,

wherein the adding the delay to the signal further includes adding the delay to the signal on the second IF signal path or the fourth IF signal path.

27. (Original) The method according to claim 26, wherein the setting the gain further includes setting the gain in part based on a predetermined criteria.

28. (Original) The method according to claim 27, wherein the predetermined criteria includes at least one of the following: a distance between a receive frequency and a transmit frequency, a regulatory rule, a temperature, a received power level, a transmit power level, and a detected interference level.

29. (Original) The method according to claim 28, further comprising storing the predetermined criteria in a memory.

30. (Original) A method for frequency translation in a frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the method comprising:

detecting if a signal is present on one of two frequency channels associated with the frequency translating repeater;

changing a frequency channel associated with the signal from the one of the two frequency channels to an other of the two frequency channels;

adding a delay to the signal to compensate for a signal detection interval and a transmitter configuration interval; and

adjusting a gain value of the signal in part based on a detected receive power level of the signal.

31. (Original) The method according to claim 30, wherein the adjusting the gain value is based on a criteria including which of the one of the two frequency channels the signal is received on, and which of the other of the two frequency channels is changed to.

32. (Original) The method according to claim 30, wherein the criteria further includes a regulatory rule for transmission.

33. (Original) The method according to claim 31, wherein the criteria further includes frequency separation between a receive frequency and a transmit frequency.

34. (Original) A method for frequency translation in a frequency translating repeater for use in a time division duplexing (TDD) radio protocol system, the method comprising:

detecting if a signal is present on one of two frequency channels associated with the frequency translating repeater and, if so, a receive power level of the signal;

converting the signal from a radio frequency (RF) signal to an intermediate frequency (IF) signal;

changing a frequency channel associated with the IF signal from the one of the two frequency channels to an other of the two frequency channels;

adding a delay to the IF signal to compensate for a signal detection interval and a transmitter configuration interval; and

adjusting a gain value of the IF signal based at least in part on the detected receive power level of the signal.

35. (Original) The method according to claim 34, wherein the detecting and the adjusting are performed respectively on a first and a second signal path.

36. (Original) The method according to claim 35, wherein the detecting further includes generating a logarithmic signal from the signal and using the logarithmic signal for the adjusting.

37. (Original) The method according to claim 36, wherein the adjusting further includes using a predetermined criteria the adjusting the gain value of the IF signal.

38. (Original) The method according to claim 19, wherein the generating further includes converting the logarithmic signal to a digital signal; and wherein the adjusting further adjusting the gain value of the IF signal using the digital signal.

39. (Currently Amended) A frequency translating repeater for use in a time division duplexing communication system, the frequency translating repeater comprising:

at least two receivers capable of receiving transmissions on at least first and second frequency channels;

at least one transmitter capable of transmitting on the first frequency channel;

at least one transmitter capable of transmitting on the second frequency channel;

a detector circuit configured to detect if a signal is present on one of two frequency channels associated with the frequency translating repeater and for detecting a receive power level of the signal;

a frequency translator configured to change a frequency channel associated with the signal from an initial one of the first and second frequency channels to a subsequent one of the first and second frequency channels;

a gain control circuit for adjusting a gain of the signal;

a delay circuit configured to add a delay to the signal to compensate for a signal detection interval, a gain adjustment interval and a transmitter configuration interval; and

a microprocessor capable of configuring the first and second frequency channels based on pre-determined parameters stored therein, wherein

configuration of a specific frequency for at least one of the first and second frequency channels is based on the pre-determined parameters, and

the pre-determined parameters include at least one of the following: regulatory transmitter power limitations, regulatory out-of-band emissions limitations, and frequency separation between the first and second frequency channels.

40. (New) The method according to claim 34, further comprising:

splitting the signal onto a first path and a second path; and

splitting the first path into a first IF signal path and a second IF signal path, and splitting the second path into a third IF signal path and a fourth IF signal path,

wherein the detecting if the signal is present further includes detecting if the signal is present on the first IF signal path or the third IF signal path,

wherein the adding the delay to the IF signal further includes adding the delay to the signal on the second IF signal path or the fourth IF signal path.

41. (New) The method according to claim 30, further comprising:

splitting the signal onto a first path and a second path; and

splitting the first path into a first IF signal path and a second IF signal path, and splitting the second path into a third IF signal path and a fourth IF signal path,

wherein the detecting if the signal is present further includes detecting if the signal is present on the first IF signal path or the third IF signal path,

wherein the adding the delay to the signal further includes adding the delay to the signal on the second IF signal path or the fourth IF signal path.